

# Search Report

## STIC Database Tracking Number 290930

To: JOSE DEES

Location: JEF-8D59

Art Unit: 2800

Monday, March 30, 2009

Patent Number: 6,297,140

From: DIANE JACKSON

Location: EIC2800

**JEF-4B68** 

Phone: (571)272-3260

diane.jackson@uspto.gov

### Search Notes

Attached are litigation search results in Lexis Nexis, and CourtLink and Questel-Orbit.

No Litigation was found for Patent Number 6,297,140.

If you have any questions, please feel free to contact me.

Thanks,

Diane



# MAR 3 0 2009

Jackson, Diane

From:

Dees, Jose

Sent:

Friday, March 27, 2009 3:48 PM

To:

STIC-EIC2800

Subject: Reissue 10/677166

Please do a litigation search for Patent No. 6,297,140.

Thanks, J Dees

lose' G. Dees lose' G. Dees r-QAS, TC 2800 571-272-1569

#### Selected file: PLUSPAT

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Coverage: 79 patenting authorities; start dates vary from 1800 forward
Abstracts/Titles in English , French & German. Increased
standardization
of Assignee/Inventor names. Added cited ref's BE , CH , NL , TR , AU ,
& JPB

For PlusPat Fact Sheet , Pricing and FAQ , see the Questel website Last update of file: 2009/03/27 (YYYY/MM/DD) 2009-13/UP (last update)

Search statement 1

# nbr/pn us6297140

PLUSPAT1 US6297137	1
PLUSPAT2 US6297138	1
PLUSPAT3 US6297139	1
PLUSPAT4 US629714	1
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PLUSPAT6 US6297141	1
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1/1 PLUSPAT -Worldwide Patents - @Questel



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US6297140 (B1) Method to plate C4 to copper stud
         US6297140 B1 20011002 [US6297140]
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      (B1) Method to plate C4 to copper stud
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      (B1) IBM (US)
      International Business Machines Corporation, Armonk NY [US]
PA0
      (B1) UZOH CYPRIAN EMEKA (US); EDELSTEIN DANIEL C (US)
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       Division of: US6251528
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      C23C-018/31 [2006-01 A L I R M JP]
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- -US6140234 [US6140234] 438678000
- -JP52-155055 [JP51155055]
- -JP3-190240 A [JP03190240]
- STG (B1) U.S. Patent (no pre-grant pub.) after Jan. 2, 2001

A method for plating a second metal directly to a first metal without utilizing a mask. A semiconductor substrate is provided including at least one metal feature and at least one insulating layer covering the metal feature and the substrate. At least one recess is formed in the at least one insulating layer thereby exposing at least a portion of the metal feature. At least one conductive barrier layer is formed over the insulating layer and the exposed

AB portion of the metal feature. A plating seed layer of a first metal is formed over the at least one barrier layer. A photoresist layer is deposited over the plating seed layer. Portions of the photoresist layer and portions of the plating seed layer outside of the at least one recess are removed. Photoresist remaining in the at least one recess is removed. A second metal is electroplated to the plating seed layer in the recess, using the barrier layer to conduct electrical current.

UP 2001-41

Search statement 2

#### .. fi fampat

Selected file: FAMPAT

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RELOADED 02/2008 Searchable bibliographic & abstracts-all family members

Search & display options for both FamPat & extended family definition Coverage: 79 patenting authorities; start dates vary from 1800 forward Abstracts/Titles in English, French & German. Increased standardization

of Assignee/Inventor names. Added cited ref's BE , CH , NL , TR , AU , & JPB

For more details , see the FamPat Fact Sheet and Questel website Last update of file: 2009/03/27 (YYYY/MM/DD) 2009-13/UP (last update)

Search statement 1

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	US6251528 B1 20010626 [US6251528]	
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	US2001032787 A1 20011025 [US20010032787]	
	JP3245122 B2 20020107 [JP3245122]	
TI	Method to plate C4 to copper stud	
PA	IBM	
PA0	International Business Machines Corporation, Armonk NY [US]	
IN	UZOH CYPRIAN EMEKA; EDELSTEIN DANIEL C	
	1998US-0004808 19980109	
	1999JP-0003342 19990108	
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	Division of: US6251528	
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       ORIGINAL (O): 428587000; CROSS-REFERENCE (X): 257E21508
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       4K024 AA09; 4K024 AA22; 4K024 AB02; 4K024 AB03; 4K024 AB04;
       4K024 AB08; 4K024 AB15; 4K024 AB17; 4K024 AB19; 4K024 BA07;
       4K024 BB12; 4K024 BC10; 4K024 FA01; 4K024 FA05; 4K024 GA16;
       4M104 BB04; 4M104 BB36; 4M104 CC01; 4M104 DD34; 4M104 DD38;
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       4M104 DD43; 4M104 DD52; 4M104 DD53; 4M104 EE06; 4M104 EE18;
       4M104 FF06; 4M104 FF17; 4M104 FF18; 4K022 AA02; 4K022 DA01;
       4K022 BA08; 4K022 AA05; 4K022 AA37; 4K022 AA41; 4K022 BA35;
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       -US5089440 [US5089440]
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      -JP3-190240 A [JP03190240]
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       -US6140234 [US6140234] 438678000
       -JP52-155055 [JP51155055]
       -JP3-190240 A [JP03190240]
       (JP11274208)
       (A)
       [19] Citation as reason for refusal of an application
CT
       - JP (A) 1991190240 [JP03190240]
       - JP (A) 1977155055 [JP52155055]
       (US6251528)
       A method for plating a second metal directly to a first metal without utilizing
       a mask. A semiconductor substrate is provided including at least one metal
       feature and at least one insulating layer covering the metal feature and the
       substrate. At least one recess is formed in the at least one insulating layer
AB
       thereby exposing at least a portion of the metal feature. At least one
       conductive barrier layer is formed over the insulating layer and the exposed
       portion of the metal feature. A plating seed layer of a first metal is formed
       over the at least one barrier layer. A photoresist layer is deposited over the
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plating seed layer. Portions of the photoresist layer and of the plating seed layer outside of the at least one recess are removed. Photoresist remaining in the at least one recess is removed. A second metal is electroplated to the plating seed layer in the recess.

(US6251528)

The present invention relates to a process for plating a conductive material to a conductive feature in and/or on a substrate.

More particularly, the present invention concerns electroplating a conductive material to a metal feature in and/or on a substrate using a highly conducting barrier film to conduct electrical current.

In particular, the present invention provides methods for electroplating a solder ball utilized in a controlled collapse chip connection (C4) process to a metal feature provided in and/or on a substrate.

Additionally, the present invention provides semiconductor structures prepared according to processes of the present invention.

Broadly, an object of the present invention is to provide a process for selectively plating metal utilizing more than one metal as an electrode.

Aspects of the present invention also provide a method for plating a second metal directly to a first metal without utilizing a mask.

(US6251528)

ADB

ICLM

One of the main advantages of the damascene process as compared to metal RIE is that it is often easier to etch an insulator as opposed to metal.

Also, insulator gap fill and planarization may be more problematic.

Another advantage of the present invention is that it may utilize a barrier metal to carry plating current.

A further advantage of the present invention is that it may eliminate plating of metal on pins.

An additional advantage of the present invention is that is may provide higher productivity as compared to known processes.

In accordance with these and other objects and advantages, the present invention provides a method for plating a second metal directly to a first without utilizing a mask.

The present invention permits the second metal to be electroplated without utilizing a mask.

An advantage of the present invention is that it provides a less expensive process that known process for producing similar results.

Additionally, the process may be less costly as compared to typical lithographically defined C4 processes. (US6251528)

1. A semiconductor structure, comprising:

a semiconductor substrate;

at least one metal feature provided in said substrate;

at least one insulating layer at least partially covering said at least one metal feature;

at least one recess located in said at least one insulating layer over said at least one metal feature;

at least one conductive barrier layer located over said at least one electrical insulating layer and over a portion of said at least one metal feature under said at least one recess, said conductive barrier layer comprising at least one nitride of tantalum and ALPHA -phase tantalum; at least one plating seed layer of a first metal located over a portion of said conductive barrier layer within said at least one recess, said seed layer and barrier layer in combination forming a continuous conductive layer; and a second metal electroplated to said seed layer within said at least one recess.

UP 2001-27

1/2 LGST - Legal Status - ©EPO

☐ 2/2 LGST - Legal Status - ©EPO

US6297140 20020625 US/CCA [COR]CERTIFICATE OF CORRECTION
PN US6297140 B1 20011002 [US6297140](B1) Granted patent as first publication
AP US38923299 19990903 [1999US-0389232]
19990903 US-API [POS; EXM]
PUBFILING DETAILS
US38923299 19990903 [1999US-0389232]

20011002 US-B1 [POS; PIF]
Granted patent as first publication
US6297140 B1 20011002 [US6297140]
20020625 US/CC-A [COR]
CERTIFICATE OF CORRECTION

ACT 20040413 US/RF-A [OPP]
REISSUE APPLICATION FILED EFFECTIVE DATE: 20031002
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Alive UP 2004-17

1/2 CRXX - US Claims Reassignations - ©CLAIMS/RRX

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PN 6,297,140 A 20011002 [US6297140]

PA International Business Machines Corp

PT C (Chemical)

20031002 REISSUE REQUESTED ISSUE DATE OF O.G.: 20040413

REISSUE REQUEST NUMBER: 10/677166

ACT EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 2812

#### Reissue Patent Number:

UP 2002-29 UACT 2004-04-13

2/2 CRXX - US Claims
Reassignations - ©CLAIMS/RRX

US6251528 20020430 CERTIFICATE OF CORRECTION

AN 3532295 PN

6,251,528 A 20010626 [US6251528] International Business Machines Corp

PA

PT .

C (Chemical)
20020430 CERTIFICATE OF CORRECTION ACT

UP 2002-18 UCOR 2002-04-30

Search statement 2 LexisNexis CourtLink

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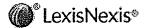
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Patent Search 6297140 3/30/2009

No cases found.

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FOCUS™ Terms Patno=6297140 Search Within Original Results (1 - 1)

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Source: Combined Source Set 10 : - Utility, Design and Plant Patents
Terms: Patno=6297140 (Edit Search | Suggest Terms for My Search)

389232 (09) 6297140 October 2, 2001

#### UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

#### 6297140

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Link to Claims Section

October 2, 2001

Method to plate C4 to copper stud

**INVENTOR:** Uzoh, Cyprian Emeka - Hopewell Junction, New York, United States (US)Edelstein, Daniel C. - New Rochelle, New York, United States (US)

**CERT-CORRECTION:** June 25, 2002 - a Certificate of Correction was issued for this patent (O.G. July 16, 2002)

**APPL-NO:** 389232 (09)

FILED-DATE: September 3, 1999

GRANTED-DATE: October 2, 2001

**ASSIGNEE-PRE-ISSUE:** September 3, 1999 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., INTERNATIONAL BUSINESS MACHINES CORPORATION OLD ORCHARD ROADARMONK, NEW YORK, 10504, Reel and Frame Number: 010421/0816

**ASSIGNEE-AT-ISSUE:** International Business Machines Corporation, Armonk, New York, United States (US), United States company or corporation (02)

LEGAL-REP: Connolly Bove Lodge & HutzAbate, Joseph P.

PUB-TYPE: October 2, 2001 - Utility Patent having no previously published pre-grant publication (B1)

PUB-COUNTRY: United States (US)

#### **REL-DATA:**

Division of Ser. No. 09/004808, January 9, 1998, GRANTED PATENT 6251528, Utility Patent having no previously published pre-grant publication (A)

**US-MAIN-CL:** 438#612

**US-ADDL-CL:** 257#E21.508, 438#613, 438#614, 438#627, 438#629, 438#637, 438#643, 438#653, 438#674, 438#675, 438#676, 438#677, 438#678, 438#687

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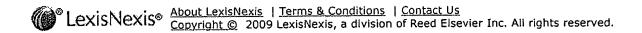
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- Use a less restrictive date range.



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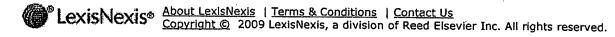
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